ABSTRACT OF THE DISCLOSURE

The semiconductor integrated circuit has a power-on resetting circuit for activating a reset signal which initializes an internal circuit, for a predetermined period after a power supply is switched on, and then inactivating the reset signal. The inactivation timing of the reset signal is changed by a timing changing circuit. Therefore, the inactivation timing which has deviated due to fluctuations in the manufacturing conditions of the semiconductor integrated circuit can be adjusted to a normal value. This consequently allows reliable initialization of the internal circuit. In general, a power-on resetting circuit utilizes the threshold voltage of transistors to generate the reset signal. Here, the inactivation timing depends on the threshold voltage of the transistors. Changing the inactivation timing corresponding to the threshold voltage of the transistors implemented makes it possible that the timing changing circuit optimally adjusts the inactivation timing of the reset signal.